WHAT IS CLAIMED IS:

1. A communication module, comprising:

a clock bus via which first and second clocks propagate exclusively, said first and second clocks respectively conforming to first and second standards which are mutually different in clock frequency, in bus arbitration, and in protocol type;

a transceiver integrated circuit from/to which first data conforming to said first standard propagate to/from an upper layer; and

a peripheral integrated circuit from/to which second data conforming to said second standard propagate to/from said transceiver integrated circuit.

2. The communication module according to claim 1, further comprising a data bus commonly used for propagating said first data and said second data.

3. The communication module according to claim 1, wherein said transceiver integrated circuit includes:

a first functional block for realizing an interface conforming to said first standard;

a second functional block for realizing an interface conforming to said second standard;

a clock pad connected to said clock bus;

a first clock line connected between said clock pad and said first functional block for propagating said first clock; and

a second clock line connected between said clock pad and said second functional block for propagating said second clock.

4. The communication module according to claim 2, wherein said transceiver integrated circuit includes:

a first functional block for realizing an interface conforming to said first standard;

a second functional block for realizing an interface conforming to said second standard;

a clock pad connected to said clock bus;

a data pad connected to said data bus;

a first clock line connected between said clock pad and said first functional block for propagating said first clock;

a second clock line connected between said clock pad and said second functional block for propagating said second clock;

a first data line connected between said data pad and said first functional block for propagating said first data; and

a second data line connected between said data pad and said second functional block for propagating said second data.

5. The communication module according to claim 1, wherein said transceiver integrated circuit includes:

a first functional block for realizing an interface conforming to said first standard;

a second functional block for realizing an interface conforming to said second standard;

a clock lead frame connected to said clock bus;

first and second clock pads;

a first clock line connected between said first clock pad and said first functional block for propagating said first clock;

a second clock line connected between said second clock pad and said second functional block for propagating said second clock;

a first wire for connecting said clock lead frame to said first clock pad; and

a second wire for connecting said clock lead frame to said second clock pad.

6. The communication module according to claim 2, wherein said transceiver integrated circuit includes:

a first functional block for realizing an interface conforming to said first standard;

a second functional block for realizing an interface conforming to said second standard;

a clock lead frame connected to said clock bus;

a data lead frame connected to said data bus;

first and second clock pads;

first and second data pads;

a first clock line connected between said first clock pad and said first functional block for propagating said first clock;

a second clock line connected between said second clock pad and said second functional block for propagating said second clock;

a first data line connected between said first data pad and said first functional block for propagating said first data;

a second data line connected between said second data pad and said second functional block for propagating said second data;

a first wire for connecting said clock lead frame to said first clock pad;

a second wire for connecting said clock lead frame to said second clock pad;

a third wire for connecting said data lead frame to said first data pad; and

a fourth wire for connecting said data lead frame to said second data pad.

7. The communication module according to claim 5, wherein

said clock lead frame has bifurcated tips,

said first wire connects one of said bifurcated tips of said clock lead frame to said first clock pad, and

said second wire connects the other of said bifurcated tips of said clock lead frame to said second clock pad.

8. The communication module according to claim 6, wherein

said clock lead frame has bifurcated tips,

said data lead frame has bifurcated tips,

said first wire connects one of said bifurcated tips of said clock lead frame to said first clock pad,

said second wire connects the other of said bifurcated tips of said clock lead frame to said second clock pad,

said third wire connects one of said bifurcated tips of said data lead frame to said first data pad, and

said fourth wire connects the other of said bifurcated tips of said data lead frame to said second data pad

9. A transceiver integrated circuit comprising:

first and second functional blocks for realizing interfaces respectively conforming to first and second standards which are mutually different in clock frequency, in bus arbitration, and in protocol type;

a clock pad;

a first clock line connected between said clock pad and said first functional block for propagating first clock conforming to said first standard; and

a second clock line connected between said clock pad and said second functional block for propagating second clock conforming to said second standard.

10. The transceiver integrated circuit according to claim 9, further comprising:

a data pad;

a first data line connected between said data pad and said first functional block for propagating first data conforming to said first standard; and

a second data line connected between said data pad and said second functional block for propagating second data conforming to said second standard.

11. A transceiver integrated circuit comprising:

first and second functional blocks for realizing interfaces respectively conforming to first and second standards which are mutually different in clock frequency, in bus arbitration, and in protocol type;

a clock lead frame;

first and second clock pads;

a first clock line connected between said first clock pad and said first functional block for propagating first clock conforming to said first standard;

a second clock line connected between said second clock pad and said second functional block for propagating second clock conforming to said second standard;

a first wire for connecting said clock lead frame to said first clock pad; and

a second wire for connecting said clock lead frame to said second clock pad.

12. The transceiver integrated circuit according to claim 11, further comprising:

a data lead frame;

first and second data pads;

a first data line connected between said first data pad and said first functional block for propagating first data conforming to said first standard;

a second data line connected between said second data pad and said second functional block for propagating second data conforming to said second standard;

a third wire for connecting said data lead frame to said first data pad; and

a fourth wire for connecting said data lead frame to said second data pad.

13. The transceiver integrated circuit according to claim 11, wherein

said clock lead frame has bifurcated tips,

said first wire connects one of said bifurcated tips of said clock lead frame to said first clock pad, and

said second wire connects the other of said bifurcated tips of said clock lead frame to said second clock pad.

14. The transceiver integrated circuit according to claim 12, wherein

said clock lead frame has bifurcated tips,

said data lead frame has bifurcated tips,

said first wire connects one of said bifurcated tips of said clock lead frame to said first clock pad,

said second wire connects the other of said bifurcated tips of said clock lead frame to said second clock pad,

said third wire connects one of said bifurcated tips of said data lead frame to said first data pad, and

said fourth wire connects the other of said bifurcated tips of said data lead frame to said second data pad.